CLAIMS

1. Modular interconnection architecture for an expandable multiprocessor machine, based on a virtual bus hierarchy, comprising a given number of multiprocessor modules (QPi) organized into nodes (Nj) and distributed on at least two interconnection levels: a first level (MI) corresponding to the interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) that connect the multiprocessor modules (QPi) to one another and handle the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCE) that connect the nodes (Nj) to one another and handle the transactions between the nodes (Nj), characterized in that the connection agents (NCSi) and the external connection nodes (NCEj) respectively have the same basic structure, the same external interface (XI), and implement the same coherency control protocol for the cache memories of the processors.

2. Architecture according to claim 1, characterized in that each external connection node (NCEj) comprises two identical connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j) receiving and filtering the transactions sent by the node (Nj) to which it is connected, and the other (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which it is connected.

3. Architecture according to claim 1, characterized in that each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

4. Architecture according to claim 2, characterized in that the connection agents

(NCS'j and NCS"j) respectively comprise an associative memory (DD'j and DD"j) with a fixed size determined as a function of the number of processors in the multiprocessor modules (HBj) to which they are connected, the state of the associative memories (DD'j and DD"j) being indicative of the presence of the last modified data blocks exported, or conversely imported.

5. Architecture according to claim 2, characterized in that the first and second head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for the blocks that are modified in their respective associative memories (DD'j and DD"j); the modified data blocks in the first connection agent (NCS'j) are exported to the requesting multiprocessor module or modules and, conversely, the modified data blocks in the second connection agent (NCS"j) are imported from the module or modules holding the blocks.

6. Architecture according to any of claims 1 through 5, characterized in that the latency of the second interconnection level (SI) is double the latency of the first interconnection level (MI).

7. Process for tracing data blocks in an interconnection architecture according to any of claims 1 through 6, characterized in that it consists, on the first level, of duplicating in the associative memories (DDi) only the modified data blocks in the cache memories of the multiprocessor modules (QPi) and of tracing only the modified blocks inside the node (Nj).

8. Process for tracing data blocks in an interconnection architecture according to any of claims 1 through 6, characterized in that it consists, on the second level (SI), of duplicating in the associative memories (DD'j and DD"J) of the connection agents (NCS' and NCS"j) of each external connection node (NCEj) only the modified blocks exported, or conversely imported, and of tracing only the modified blocks exported, or conversely imported, between each node (Nj) of the machine.

9. Process for expanding the capacity of a machine comprising a first given number

of processors on a first level (MI) organized into a first given number of multiprocessor modules (QPi) and capable of being inserted into an interconnection architecture according to any of claims 1 through 6, characterized in that it consists of disconnecting one of the first-level multiprocessor modules (QPi) from its connection agent (NCSi) and of connecting, via this freed connection agent, a second given number of processors organized into a second given number of multiprocessor modules, also capable of being inserted into an interconnection architecture according to any of claims 1 through 6.

10. Process according to claim 9, characterized in that, the second given number of processors being organized into a second given number of multiprocessor modules on the second level (SI), it consists of connecting it to the connection agent (NCSi) of the first given number of processors on the first level (MI) through one of the connection agents (NCS"j) on the second level.

11. Process according to claim 10, characterized in that, the second given number of processors also being on the first level (MI), it consists of connecting the respective connection agents (NCS') to the first and second given numbers of processors, the second level (SI) being reduced to a single link.

12. Expandable multinode multiprocessor machine, characterized in that it comprises an interconnection architecture according to any of claims 1 through 6.

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